TPS6420xEVM-023

User's Guide

October 2003

PMP Portable Power

SLVU093

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3.3 V to 6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the TPS6420xEVM-023 evaluation module (EVM). This EVM contains Texas Instruments high-efficiency non-synchronous buck controller that is configured to provide a regulated 3.3-V output voltage and up to 2 A of current. The users guide includes EVM specifications, test results, schematic diagram, bill of materials (BOM), and recommended test setup.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – EVM Operation
- Chapter 3 – Board Layout
- Chapter 4 – Bill of Materials and Schematic

Related Documentation From Texas Instruments

SLVS485 − TPS6420x data sheet

If you need Assistance

Contact your local TI sales representative.

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This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Trademark

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Chapter 1

Introduction

This chapter contains background information for the TPS6420xEVM-023 evaluation module.

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1.1 Background

This TPS6420xEVM uses a TPS64202 step down controller, external p-channel FET, and Schottky diode. Although the TPS64202 input voltage range is 1.8 V to 6 V, this EVM was configured to provide 2 A at 3.3 V_{OUT}, so the input voltage is limited to 3.3 V to 6 V. The goal of the EVM is to demonstrate the small size of the TPS6420x power supply solution and provide flexibility in interchanging the supporting passive components.

The TPS64202 was selected for this application because unlike the other members of the TPS6420x family, the TPS64202's switching frequency is determined by its minimum off time which, for applications where $V_I \cong V_O$, results in a high switching frequency and thus small inductor. Table 1−1 below aids in selecting the correct TPS6420x device.

Table 1−1. Device Summary

Input to Output Voltage Ratio	Switching Frequency Determined By	Proposed Device For High Switching Frequency	Proposed Device For Low Switching Frequency
$V_I >> V_O$ (e.g. V_I = 5 V V_O = 1.5 V)	Minimum on-time	TPS64203	TPS64200, TPS64201
$V_I \approx V_O$ (e.g. V_I = 3.8 V V_O = 3.3 V)	Minimum off-time	TPS64202	TPS64200, TPS64201

1.2 Performance Specification Summary

Table 1−2 provides a summary of the TPS6420xEVM performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1−2. Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Unit
Input voltage range	TPS64202EVM	3.3		6	V
Output voltage	TPS64202EVM		3.3		V
Output current		0		2	A

1.3 Modifications

The primary goal of this EVM is to demonstrate operation of the TPS6420x in a power supply solution. To facilitate user customization of the EVM, the board was designed with 603 or larger sized components, spaced further apart than necessary. So, a real implementation would likely occupy less total board space.

Any of the TPS6420x ICs can be placed on the EVM. In addition, the EVM has the following characteristics to allow user customization:

❑ Two PMOS control FET footprints: SOT23 (top) and 1206-8 ChipFET (bottom)

❑ Two Schottky diode footprints: Powermite® (top) and SMA (bottom)

- Large inductor area under removable solder mask
- Extra input and output capacitor pads
- Resistors R6 and R7 can be left open and R5 can be shorted (by a 0 Ω resistor) to allow current sensing by Q1's $r_{DS(on)}$.
- Resistor R8 and capacitor C7 can be populated to provide an RC snubber which dampens the oscillations and resulting EMI produced at the switch node when the device operates in discontinuous mode.
- The TPS6420x family of devices work best using an output capacitor with between 50 to 150 mΩ of ESR. However, they will work with low ESR ceramic output capacitors if a large resistor is placed from the SW node to the FB node as explained on the last page of the datasheet application section. Resistor R8 can be used as this large resistor since one side already connects to the SW node, if the other side is manually connected to the FB node using a small wire.

Changing components can improve or degrade EVM performance. For example, using a FET with higher $r_{DS(on)}$ and/or an inductor with larger dc resistance will lower the efficiency of the solution. In addition, using a FET in a larger package with larger gate capacitance will likely lower efficiency since the TPS6420x's gate drive limited to 150 mA, would have difficulty driving a larger gate capacitance.

Chapter 2

EVM Operation

This chapter describes how to properly test the TPS64202 using the TPS6420xEVM.

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2.1 Input/Output Connect

The EVM connection points are described in the following paragraphs.

2.1.1 J1−Vin

This is the positive connection to the input power supply. The leads to the input supply should be twisted and kept as short as possible.

2.1.2 J2−GND

This is the return connection to the input power supply.

2.1.3 JP1−Enable

This is the enable pin of the device. The enable pin is pulled up to Vin by an onboard pullup resistor. Placing a jumper across pins 2−3 of J1 shorts the enable pin to GND; thereby enabling the device. Placing a jumper across pins 1−2 of J1 connects the enable pin to Vin and disables the device.

2.1.4 J3−Vout

This is the positive output for the device.

2.1.5 J4−GND

This is the return connection for the load.

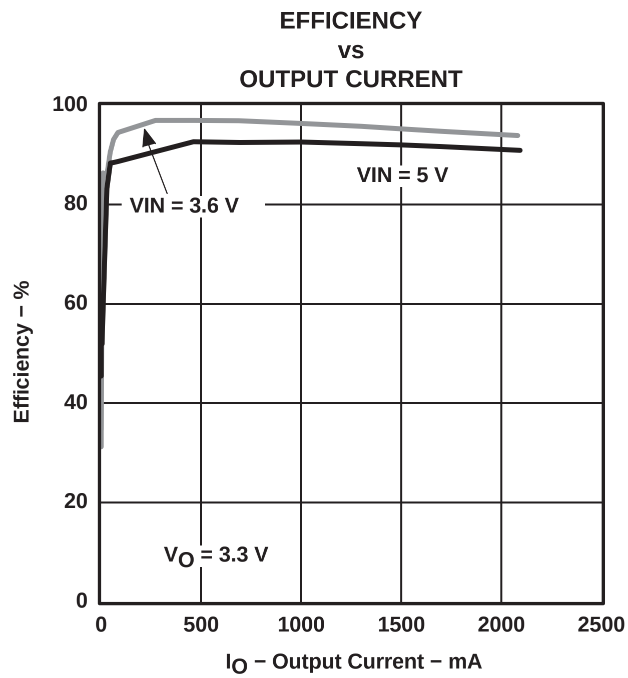
2.2 Test Setup

The absolute maximum input voltage is 7 V. The TPS62402, with V_O = 3.3 V, is designed to operate with a maximum input voltage of 6 V. Connect a power supply with output voltage between 3.3 V and 6 V and current limit set to at least 1.3 times the expected maximum output current, or for this EVM, 2.6 A. Short pins 2−3 on jumper JP1 (labeled ON) to enable the device. Connect a load not to exceed 2.0 A to the output of the EVM.

2.3 Test Results

Below are the efficiency results using this EVM:

Figure 2−1. TPS64202 Efficiency



Chapter 3

Board Layout

This chapter provides the TPS6420xEVM board layout and illustrations.

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3.1 Layout

Board layout is critical for all switch mode power supplies. Figures 3−1, 3−2, and 3−3 show the board layout for the HPA023 PWB. The switching nodes with high frequency noise are isolated from the noise sensitive feedback circuitry and careful attention has been given to the routing of high frequency current loops. Refer to the data sheet for more specific layout guidelines.

Figure 3−1. Top Assembly Layer

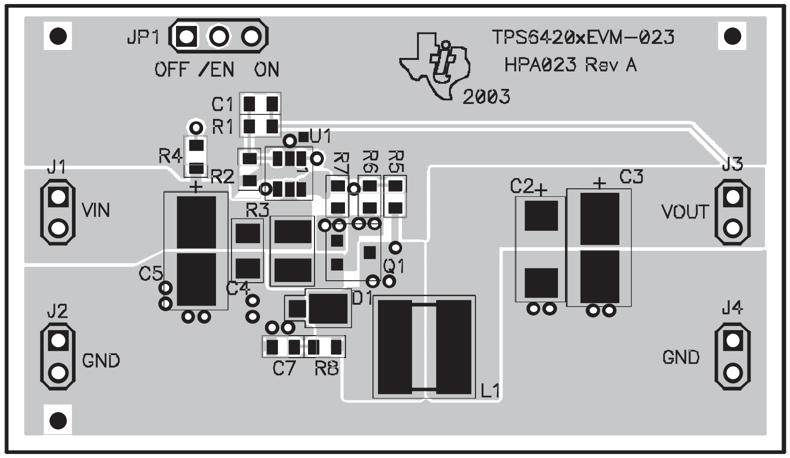


Figure 3−2. Top Layer Routing

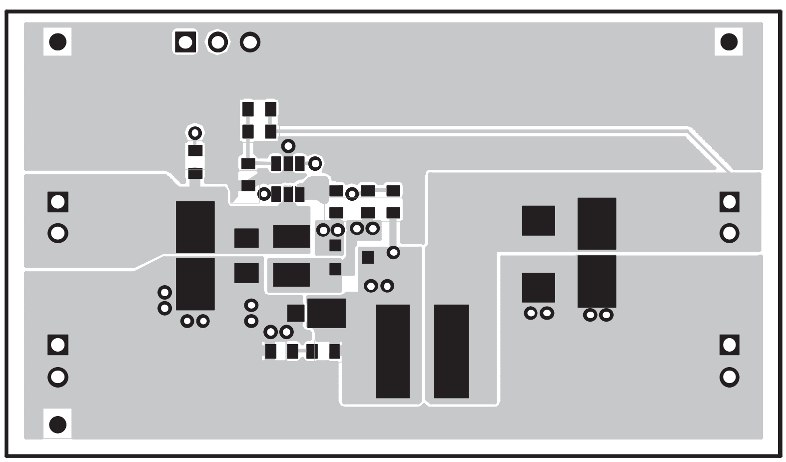
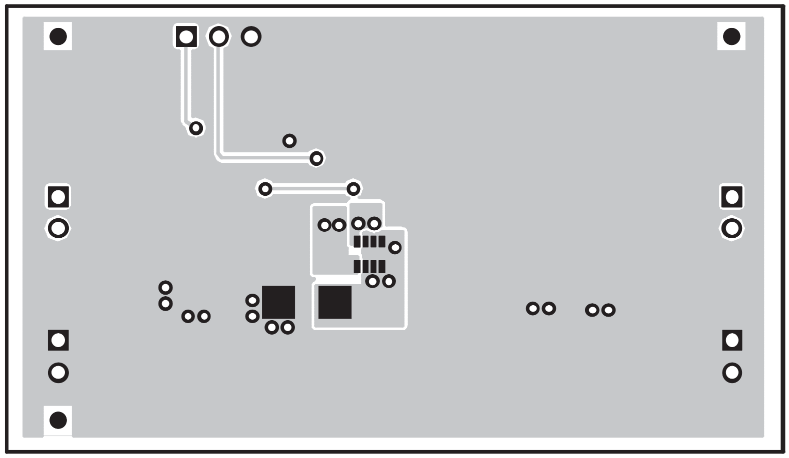


Figure 3−3. Bottom Layer Routing



Chapter 4

Bill of Materials and Schematic

This chapter provides the TPS6420xEVM-023 bill of materials and schematic.

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4.1 Bill of Materials

Table 4−1. Bill of Materials

Count	RefDes	Description	Size	MFR	Part Number
1	C1	Capacitor, ceramic, 4.7 µF, 50 V, C0G, ±10%	603	TKD	C1608X7R1H4R7DT
1	C2	Capacitor, POSCAP, 4.7 µF, 6.3 V, 100 mΩ, 20%	6032(C)	Sanyo	6TPA47M
1	C3, C5	Capacitor, Multi-pattern, 603-D case	7343 (D)		
1	C4	Capacitor, ceramic, 10 µF, 10 V, X7R, ±10%	1206	TDK	C3216X7R1A106KT
0	C7	Capacitor, ceramic, XXX µF, XX V	603		
1	D1	Diode, Schottky, 1 A, 20 V	457-04	On Semi	MBRM120
4	J1, J2, J3, J4	Header, 2 pin, 100 mil spacing, (36-pin strip)	0.100 x 2”	Sullins	PTC36SAAN
1	JP1	Header, 3 pin, 100 mil spacing, (36-pin strip)	0.100 x 3”	Sullins	PTC36SAAN
1	L1	Inductor, SMT, 5 µH, 2.9 A, 24 mΩ	0.264x0.264	Sumida	CDRH6D38−5R0
1	Q1	MOSFET, Pch, −20 V, −3.5 A, 68 mΩ	SOT23	Siliconix	Si2323
1	R1	Resistor, chip, 619 kΩ, 1/16 W, 1%	603	Std	Std
1	R2	Resistor, chip, 356 kΩ, 1/16 W, 1%	603	Std	Std
1	R3	Resistor, chip, 0.033 Ω, 1/4 W, 1%	1210	Std	Std
1	R4	Resistor, chip, 100 kΩ, 1/16 W, 1%	603	Std	Std
1	R5	Resistor, chip, XX Ω, 1/16 W	603		
1	R6, R7	Resistor, chip, 0 Ω, 1/16 W, 1%	603	Std	Std
1	R8	Resistor, chip, XX Ω, 1/16 W, 1%	603		
1	U1	IC, Step-down controller	SOT23−6	Texas Instruments	TPS64202DBV
1	—	PCB, 2.42 In x 1.395 In x 0.062 In		Any	HPA023
1	—	Shunt, 100 mil, black	0.100	3M	929950−00

4.2 Schematic

Figure 4−1. TPS6420xEVM Schematic